AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-97 (Canceled)

98. (Currently Amended) A home video game system for use with a television type monitor display device, ~~said system contained, at least in part, in a housing having an insertion port for receiving removable memory,~~ comprising:

a game program processing unit for executing at least a portion of a videographics game program that includes instructions for displaying polygon-based 3D objects; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects from said game program processing unit, the programmable graphics processor programmed to process pixel data for rendering one or more portions of polygon-based 3D objects for display on said television type monitor display.

99. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor is a coprocessor that is responsive to specific instructions used for rendering polygon-based 3D objects.

100. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor is a pipelined processor.

101. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes a high speed multiplier circuit.

102. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes embedded RAM cache memory.

103. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes graphics geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

104. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes at least an Arithmetic Logic Unit and a plurality of registers for executing instructions for performing rotation and/or scaling of a polygon-based graphic object to be displayed.

105. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

106. (Previously Presented) A home video game system as set forth in claim 105 wherein the multiplier performs multiply operations using at least 16-bit length operands.

107. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

108. (Previously Presented) A home video game system as in claim 98 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

109. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor is programmed to perform texture mapping operations.

110. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

111. (Previously Presented) A home video game system as in claim 98 having a set of instructions for programming the programmable graphics processor unit for rendering 3D graphic objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

112. (Previously Presented) A home video game system as in claim 98 having a set of instructions for programming the programmable graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

113. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

114. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

115. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

116. (Previously Presented) A home video game system as in claim 98 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

117. (Currently Amended) A home video game system for use with a television type display device ~~said system contained at least in part in a housing having an insertion port for~~

~~receiving a removable memory storage device storing video game program instructions and/or data,~~ comprising:

a game program processor; and

a graphics processor for rendering at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, said graphics processor including a programmable processor having embedded RAM cache memory.

118. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

119. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor is a pipelined processor.

120. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor includes a high speed multiplier circuit.

121. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor includes a plurality of data storage registers.

122. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor includes graphic geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

123. (Previously Presented) A home video game system as in claim 122 wherein the geometry transformation circuitry includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

124. (Previously Presented) A home video game system as set forth in claim 123 wherein the multiplier circuit performs multiply operations using at least 16-bit length operands.

125. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

126. (Previously Presented) A home video game system as in claim 117 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

127. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor is programmed to perform texture mapping operations.

128. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

129. (Previously Presented) A home video game system as in claim 117 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

130. (Previously Presented) A home video game system as in claim 117 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

131. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

132. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

133. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

134. (Previously Presented) A home video game system as in claim 117 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

135. (Currently Amended) A home video game system, for use with a television type monitor display device, ~~said system having a housing and an insertion port in the housing for receiving removable program memory,~~ comprising:

a game program processing unit for executing at least a portion of a videographics program that includes instructions for drawing one or more trapezoids for constructing and displaying polygon-based 3D graphic objects;

a video RAM for providing video frame data to a display device; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects, the graphics processor programmed to process pixel data for subsequent transfer to said video RAM corresponding to one or more portions of polygon-based objects to be displayed.

136. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

137. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor is a pipelined processor.

138. (Previously Presented) A home video game system as in claim 135 wherein the transfer of pixel data to video RAM is a direct memory access (DMA) type transfer.

139. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes a high speed multiplier circuit.

140. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes embedded RAM cache memory.

141. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

142. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

143. (Previously Presented) A home video game system as set forth in claim 142 wherein the multiplier performs multiply operations using at least 16-bit length operands.

144. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

145. (Previously Presented) A home video game system as in claim 135 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

146. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor is programmed to perform texture mapping operations.

147. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

148. (Previously Presented) A home video game system as in claim 135 having a set of instructions for programming the graphics processor unit for rendering 3D graphic objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

149. (Previously Presented) A home video game system as in claim 135 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

150. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

151. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

152. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

153. (Previously Presented) A home video game system as in claim 135 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

Claims 154-185 (canceled)

186. (Currently Amended) In a home video game system ~~having a housing and an insertion port in the housing for receiving a removable memory for storing a video game program, said system~~ for use with a television type monitor, said home video game system including a game program processor for executing at least a portion of a video graphics program

that includes instructions for displaying polygon-based 3D objects, a programmable graphics processor and a video RAM for providing video frame data to a television type monitor display device, a method for performing operations for rotation and/or scaling of polygon-based 3D graphic objects to be displayed on the display device, comprising the steps of:

computing display screen position coordinates for a rotated and/or scaled polygon-based object; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object to the video RAM.

187. (Currently Amended) A home video game system for use with a television type monitor display device~~, said system contained at least in part in a housing having an insertion port for receiving a removable memory storage device storing video game program instructions and/or data~~, comprising:

a separate game program processor;

a graphics processor for rendering at least one or more ~~portioning~~ portions of a polygon-based 3D graphic object for displaying on the display device; and

a CD ROM reader device, wherein at least a portion of program instructions and/or graphics data used in rendering a 3D graphic object is accessed from a CD ROM.

188. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

189. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor is a pipelined processor.

190. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor includes a high speed multiplier circuit.

191. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor includes a plurality of data storage registers.

192. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor includes geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

193. (Previously Presented) A home video game system as in claim 192 wherein the geometry transformation circuitry includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

194. (Previously Presented) A home video game system as set forth in claim 193 wherein the multiplier circuit performs multiply operations using at least 16-bit length operands.

195. (Currently Amended) A home video game system as in claim 187 wherein the graphics processor is programmed to rotate an array of X, Y and Z coordinate data corresponding to ~~polygon~~ vertex points of a polygon-based 3D graphics object.

196. (Previously Presented) A home video game system as in claim 187 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

197. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor is programmed to perform texture mapping operations.

198. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

199. (Previously Presented) A home video game system as in claim 187 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

200. (Previously Presented) A home video game system as in claim 187 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

201. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

202. (Currently Amended) In a home video game system ~~having an insertion port for receiving removable memory for storing video game program data and/or instructions~~ for use with a television display device, said system including a game program processor and a programmable pipelined graphics processor, a method for performing operations for rotation and/or scaling of polygon-based 3D graphic objects to be displayed on a raster scan type display device, comprising the steps of:

computing bit mapped display screen position object coordinates for a rotated and/or scaled polygon-based object to be displayed; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object to a video display RAM.

203. (Previously Presented) The method as in claim 202 wherein the writing of pixel information is accomplished via a direct memory access (DMA) operation.

204. (Currently Amended) In a home video game system[[,]] used with a television type monitor, the game system having a game program processor and a programmable graphics processor, the graphics processor having circuitry including a plurality of storage registers for increasing computational speed when processing 3D graphic geometric transformation

operations, a method of producing 3D type graphics display effects utilizing rotated ~~and/or scaled~~ polygon-based objects, comprising the steps of:

using a plurality of storage registers of the graphics processor as a rotation matrix for computing rotated coordinator of vertices of polygon-based graphic objects;

providing said graphics processor with X, Y and Z vertex coordinate information relating at least in part to a polygon based 3D graphic object; ~~and~~

computing new X, Y and Z coordinate values corresponding to a rotated 3D graphic object using said rotation matrix; and

writing pixel color information corresponding to the rotated ~~and/or scaled~~ polygon-based object into a video display RAM.

205. (Previously Presented) The method as in claim 204 wherein the writing of pixel information is accomplished via a DMA operation.

Claims 206-223 (canceled)